BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/955,007	09/10/2001	Viktor Andrew Tymchenko	2207/353102	7863

7590 06/29/2004

John C. Altmiller
KENYON & KENYON
1025 Connecticut Avenue, N.W.
Washington, DC 20036

EXAMINER	
VOELTZ, EMANUEL T	

ART UNIT	PAPER NUMBER
2121	

DATE MAILED: 06/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/955,007	TYMCHENKO, VIKTOR ANDREW	
	Examiner	Art Unit	
	Emanuel T. Voeltz	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATE
UNITED STATES PATENT AND TRADEMARK OFFI
WASHINGTON, D.C. 20
www.uspto.

Examiner's Detailed Office Action

This action is in response to patent application number 09/955,007, filed January 22, 2002.

Claims 1-30 have been examined.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-13 and 15-30 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,713,030, granted to Evoy.

Regarding claim 1,

A computer system comprising: a processor having an input (see Evoy, figure 3, Processor Chip 102), and responsive to a signal at said input (see Evoy, figure 3, input to Processor Chip 114a), reducing a power consumption of said processor (see Evoy, figure 3, Clock Generator 114); and a power reduction circuit coupled to said input of said processor and providing a signal to said input of said processor in response to a failure condition affecting said processor such that the power consumption of said processor is periodically reduced (see Evoy, figure 3, Control Unit 110).

Regarding claim 2,

A computer system according to claim 1, wherein a first signal level of the signal at the input of the processor stops an internal clock of the processor.

Regarding claim 3,

A computer system according to claim 1, wherein said signal provided to said input of said processor in response to said failure condition comprises a periodic signal including at least a first signal level and a second signal level (see Evoy, figure 3, Clock Generator 114).

Regarding claim 4,

A computer system according to claim 1, further comprising a cooling fan directing air toward said processor, wherein said failure condition affecting said processor corresponds to a reduced performance of said cooling fan (see Evoy, figure 4, Fan 124).

Regarding claim 5,

A computer system according to claim 4, said power reduction circuit including a signal generator generating said periodic signal (see Evoy, figure 3, Control Unit 110 and Clock Generator 114).

Regarding claim 6,

A computer system according to claim 5, wherein said signal generator includes inputs corresponding to characteristics of said generated periodic signal (see Evoy, figure 3, Control Unit 110 and Clock Generator 114).

Regarding claim 7,

A computer system according to claim 5, wherein said signal generator includes an input corresponding to a duty cycle of said generated periodic signal and an input corresponding to a frequency or a period of said generated periodic signal (see Evoy, figure 3, Control Unit 110 and Clock Generator 114).

Regarding claim 8,

A computer system according to claim 1, wherein said power reduction circuit detects a temperature of said processor, wherein said failure condition affecting said processor is detected when said detected temperature of said processor is above a predetermined temperature (see Evoy, figure 3, Thermistor Circuit 116 and Comp. Circuit 118).

Regarding claim 9,

A computer system according to claim 1, wherein said power reduction circuit includes a sensor detecting a temperature of said processor, wherein said failure condition affecting said processor is detected when said sensed temperature of said processor is above a predetermined temperature (see Evoy, figure 3, Thermistor Circuit 116 and Comp. Circuit 118).

Regarding claim 10,

A computer system according to claim 9, wherein said sensor comprises a temperature sensor embedded in a heat sink attached to said processor (see Evoy, figure 4, Heat Sink 126).

Regarding claim 11,

A computer system according to claim 3, said power reduction circuit including a switch providing said periodic signal to said input in response to a presence of said

failure condition affecting said processor, said switch providing said second signal level to said input in response to an absence of said failure condition affecting said processor (see Evoy, figure 3, Control Unit 110 and Clock Generator 114).

Regarding claim 12,

A computer system according to claim 3, said power reduction circuit including a multiplexor providing said periodic signal to said input in response to a presence of said failure condition affecting said processor, said multiplexor providing said second signal level to said input in response to an absence of said failure condition affecting said processor (see Evoy, figure 3, Control Unit 110 and Clock Generator 114).

Regarding claim 13,

A computer system according to claim 1, wherein said failure condition affecting said processor is a thermal temperature condition corresponding to an overtemperature condition of said processor at or near said processor (see Evoy, figure 3, Thermistor Circuit 116 and Comp. Circuit 118).

Regarding claim 15,

An apparatus for reducing a power consumption of a processor, comprising: a signal generator generating a failure condition signal indicating a failure condition affecting said processor; and a power reduction circuit responsive to said failure condition signal and providing a periodic signal for periodically reducing a power consumption of said processor (see rejection to claim 1 above).

Regarding claim 16,

An apparatus according to claim 15, wherein said apparatus includes said processor, and said processor has a power consumption reduction input, wherein said

power reduction circuit provides said periodic signal to said power consumption reduction input of said processor in response to said failure condition signal (see rejection to claim 3 above).

Regarding claim 17

An apparatus according to claim 16, wherein an internal clock of the processor is stopped in response to the power consumption reduction input of the processor (see rejection to claim 2 above).

Regarding claim 18,

An apparatus according to claim 15, further comprising a cooling fan directing air toward said processor, wherein said failure condition affecting said processor corresponds to a reduced performance of said cooling fan (see rejection to claim 4 above).

Regarding claim 19,

An apparatus system according to claim 15, said power reduction circuit including a signal generator generating said periodic signal (see rejection to claim 5 above).

Regarding claim 20,

An apparatus according to claim 15, wherein said power reduction circuit includes a sensor detecting a temperature of said processor, wherein said failure condition affecting said processor is detected when said sensed temperature of said processor is above a predetermined temperature (see rejection to claim 8 above).

Regarding claim 21,

An apparatus according to claim 20, wherein said sensor comprises a temperature sensor embedded in a heat sink attached to said processor (see rejection to claim 10 above).

Regarding claim 22,

An apparatus according to claim 16, said power reduction circuit including a switch providing said periodic signal to said power condumption reduction input in response to a presence of said failure condition affecting said processor (see rejection to claim 11 above).

Regarding claim 23,

An apparatus according to claim 16, said power reduction circuit including a multiplexor providing said periodic signal to said power consumption reduction input in response to a presence of said failure condition affecting said processor (see rejection to claim 12 above).

Regarding claim 24,

An apparatus according to claim 15, wherein said failure condition affecting said processor is a thermal failure condition corresponding to an overtemperature condition of said processor at or near said processor (see rejection to claim 13 aboe).

Regarding claim 25,

A method of reducing a power consumption of a processor, comprising steps of: detecting a failure condition affecting said processor; and periodically reducing a power consumption of said processor in response to said step of detecting said failure condition (see rejection to claim 1 above).

Regarding claim 26,

A method according to claim 25, wherein said step of periodically reducing the power consumption of said processor comprises periodically stopping an internal clock of said processor (see rejection to claim 2 above).

Regarding claim 27,

A method according to claim 25, further comprising a step of measuring a temperature at or near said processor and providing said signal indicating a failure condition affecting said processor in response to said measured temperature (see rejection to claim 1 above).

Regarding claim 28,

A method according to claim 25, further comprising a step of providing said signal indicating a failure condition affecting said processor in response to a reduction in performance of a cooling fan (see rejection to claim 4 above).

Regarding claim 29,

A method according to claim 25, wherein said failure condition affecting said processor corresponds to an overtemperature condition of said processor at or near said processor (see rejection to claim 13 above).

Regarding claim 30,

A method according to claim 25, wherein said failure condition affecting said processor is a thermal failure condition affecting a temperature of said processor (see rejection to claim 1 above).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Evoy in view of U.S. Patent 6,141,762, granted to Nicol et al.

Regarding claim 14

A computer system according to claim 1, said computer system further comprising: at least one additional processor each having an input (see Nicol et al., figure 2, Processing Elements 101-104), wherein a power consumption of each processor is reduced in response to a first signal level of the input of that processor and is not reduced in response to a second signal level of the input of that processor (see Evoy, figure 3, input to Processor Chip 114a); and at least one additional power reduction circuit, each said additional power reduction circuit respectively corresponding to each said at least one additional processor and providing a signal to said input of said corresponding processor in response to a failure condition affecting the corresponding processor (see Nicol et al., figure 2, Processing Elements 101-104), wherein said signal provided to said input of said corresponding processor comprises a periodic signal including at least the first signal level and the second signal level (see Evoy, figure 3, Clock Generator 114).

The patent to Evoy sets forth a thermal management device and method for a single computer processor as seen from claims 1-13 above. Evoy, however, fails to disclose the use of redundant processors. The patent to Nicol et al. teaches the use of multi-processor elements in a power reduction system using redundant processors. It would have been obvious to one of ordinary skill in the art to use the thermal management system of Evoy using redundant processors as taught by Nicol et al. because thermal management of redundant processor systems would be just as necessary as they are for single processor systems. Many applications in the computing environment are turning to the use of redundant processors.

Prior Art of Record

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The various patents are cited for showing the general state of the art in thermal management of processors.

Correspondence Information

Any inquiries concerning this communication or earlier communications from the examiner should be directed to **Emanuel Todd Voeltz** who may be reached via telephone at

(703) 305-4563. The examiner can normally be reached Monday through Friday between the

hours of 8:00 a.m. and 5:00 p.m. eastern standard time.

If you need to send an Official facsimile transmission, please send it to **(703) 872-9306**. If you would like to send a Non-Official (draft) facsimile transmission the fax

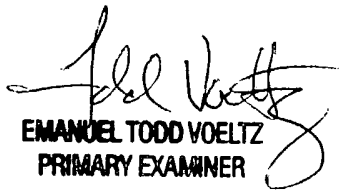
is **(703) 746-5104**. If attempts to reach the examiner by telephone are unsuccessful, the Examiner's Supervisor, **Anthony Knight**, may be reached at **(703) 308-3179**.

Any response to this office action should be mailed too: **Director of Patents and Trademarks Washington, D.C. 20231**.

Moreover, hand-delivered responses should be delivered to the Receptionist, located

on the **fourth floor of Crystal Park 11, 2121 Crystal Drive Arlington, Virginia**.

Emanuel Todd Voeltz
Primary Patent Examiner
Art Unit 2121
United States Department of Commerce
Patent & Trademark Office



Notice of References Cited	Application/Control No. 09/955,007	Applicant(s)/Patent Under Reexamination TYMCHENKO, VIKTOR ANDREW	
	Examiner Emanuel T. Voeltz	Art Unit 2121	Page 1 of 2

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,483,102	01-1996	Neal et al.	257/712
	B	US-5,574,667	11-1996	Dinh et al.	700/300
	C	US-5,612,677	03-1997	Baudry, Jean-Jerome C.	340/584
	D	US-5,713,030	01-1998	Evoy, David Ross	713/322
	E	US-5,805,403	09-1998	Chemla, Guy	361/103
	F	US-5,835,885	11-1998	Lin, Huo-Yuan	702/99
	G	US-5,940,786	08-1999	Steeby, Jon	702/132
	H	US-6,014,611	01-2000	Arai et al.	702/132
	I	US-6,141,762	10-2000	Nicol et al.	713/300
	J	US-6,226,556 B1	05-2001	Itkin et al.	700/21
	K	US-6,363,490 B1	03-2002	Senyk, Borys S.	713/300
	L	US-6,393,374 B1	05-2002	Rankin et al.	702/132
	M	US-6,415,388 B1	07-2002	Browning et al.	713/322

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N	JP358001202A	01-1983	Japan	Nagashima	-
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Notice of References Cited	Application/Control No. 09/955,007	Applicant(s)/Patent Under Reexamination TYMCHENKO, VIKTOR ANDREW	
	Examiner Emanuel T. Voeltz	Art Unit 2121	Page 2 of 2

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,470,238 B1	10-2002	Nizar et al.	700/299
	B	US-6,470,289 B1	10-2002	Peters et al.	702/132
	C	US-6,510,400 B1	01-2003	Moriyama, Shuichi	702/132
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

PAT-NO: JP358001202A

DOCUMENT-IDENTIFIER: JP 58001202 A

TITLE: CONTROLLER

PUBN-DATE: January 6, 1983

INVENTOR-INFORMATION:
NAME
NAGASHIMA, MASARU

ASSIGNEE-INFORMATION:

NAME	COUNTRY
FUJI ELECTRIC CO LTD	N/A

APPL-NO: JP56098333

APPL-DATE: June 26, 1981

INT-CL (IPC): G05B009/02

US-CL-CURRENT: 361/94

ABSTRACT:

PURPOSE: To reduce the power consumption more at power failure for a controller inporporated in a processor, by increasing the period of an interruption time at power failure and its waiting time.

CONSTITUTION: The system in provided with a power failure clock CL<SB>2</SB> and a clock switching circuit 9. When a power failure is detected with a power failure detecting circuit 5, a detection signal DE is given to a clock switching circuit 9, which switches the clock of a clock generating circuit 1 from CL<SB>1</SB> to CL<SB>2</SB>. The period of the clock CL<SB>2</SB> is taken longer than the period of the clock CL<SB>1</SB>, resulting that the WAIT

state of a microprocessor is ketp longer, allowing to reduce the power consumption. Further, the signal DE is given to the microprocessor 2 via an I/O device 4, allowing the processor 2 to reduce the power consumption more with the power failure processing which has shorter processing time than the normal processing.

⑲ 日本国特許庁 (JP)　　⑪ 特許出願公開

⑫ 公開特許公報 (A)　　昭58—1202

⑤1Int. Cl.³　識別記号　庁内整理番号　⑬公開　昭和58年(1983)1月6日
G 05 B 9/02　6846—5H

発明の数　1
審査請求　未請求

(全 3 頁)

---

⑤4制御装置

川崎市川崎区田辺新田1番1号
富士電機製造株式会社内

⑳特　願　昭56—98333
㉒出　願　昭56(1981)6月26日

㉑発 明 者　長島優

㉑出 願 人　富士電機製造株式会社
川崎市川崎区田辺新田1番1号

㉔代 理 人　弁理士　並木昭夫　外1名

明　細　書

1. 発明の名称

制御装置

2. 特許請求の範囲

平常時には所定周期の割込信号によつて起動され、所定の処理動作が終了すると待機状態となり、次の割込信号で該待機状態を解除して所定の処理動作を行ない、停電時には平常時とは別の予備電源から電力の供給を受けて平常時と同様の手順にて動作を行なう処理装置を有してなる制御装置において、前記割込信号の時間周期を平常時と停電時とに応じて切替える手段を設け、停電時には該手段によつて割込信号の時間周期を平常時よりも長くすることにより、前記処理装置の待機時間を長くするようにしたことを特徴とする制御装置。

3. 発明の詳細な説明

この発明は常時は交流電源によつて動作し、停電時にはバツテリなどによつて動作するマイクロプロセツサ等の処理装置を用いた制御装置、特にその制御装置における停電時の消費電力低減化方式に関する。

一般にバツテリなどによつて停電補償を行なう装置においては、補償時間とバツテリ容量などの関係から、停電補償時の消費電力は極力少ないことが望まれる。

第1図は例えばマイクロプロセツサを用いた制御装置の従来例を示すブロック図、第2図はその動作を説明するための流れ図である。

第1図において、1はクロツク発生器、2はマイクロプロセツサ、3はＷＡＩＴ(待機)回路、4は入出力装置(Ｉ／Ｏ)、5は停電検出回路、6は電源回路、7はバツテリ、8は切替回路である。

クロツク発生回路1から一定周期毎に発せられるインタラプト(割込み)信号ＩＮによつてマイクロプロセツサ2が起動されると(①)、マイクロプロセツサ2はこのインタラプト信号ＩＮを受け付けて以後の割込みを無効にする(②)。マイクロプロセツサ2は所定のプログラムにもとづいて所定の処理を行ない(③)、ＷＡＩＴ命令を実

行すると（④）、データバスＤＢ、アドレスバスＡＢ，Ｉ／Ｏ（入出力装置）４を介してＷＡＩＴ命令信号ＷＴＩがＷＡＩＴ回路３へ送られる。マイクロプロセッサ２は該回路３からのＷＡＩＴ信号ＷＴによつてＷＡＩＴ状態になるとともに、次のインタラプト信号ＩＮを受付け可能状態にして（⑤）、割込み要求があるか否かを調べ（⑥）、割込み要求があれば②に戻つて上記と同様の動作を繰り返し、なければ次の要求があるまで待機する。マイクロプロセッサ２がＷＡＩＴ状態にある場合の消費電力は他の動作状態に比べて少なく、したがつて上記の如くすることによつて消費電力を低減することができる。ところで、このような処理動作を行なうマイクロプロセッサ２は平常時は交流電源回路６からの電力により動作しているが、停電検出回路５にて停電が検出されると、電源６を切替回路８によつてバッテリ７側に切替え、該バッテリ７より電力を供給する。このため、マイクロプロセッサ２は停電時にも上記と同様にしてプログラムを実行し、所定の処理を行なうことができる。しかし、この方式では通電時と停電時の消費電力は同じであり、したがつて停電補償時間を長くするためにはバッテリ容量を増す必要がある。しかし、容量を増大することはスペースが大きくなり、かつ充電回路が複雑になるという問題がある。

したがつて、この発明の目的は、マイクロプロセッサ等の処理装置を内蔵する制御装置の停電時における消費電力をより一層低減することにある。

上記の目的は、この発明によれば、定周期割込信号によつて動作し、停電時にはバッテリ補償によつて駆動されてなる処理装置を内蔵した制御装置の停電時における割込時間周期を長くし、処理装置の待機時間を長くする、つまり低消費電力時間を長くすることにより達成される。

以下、この発明の実施例を図面を参照して説明する。

第３図はこの発明の実施例を示すブロック図、第４図は第３図の動作を説明する流れ図である。なお、第１，２図と同じものについては同一の符号を付して示している。

これらの図からも明らかなように、この発明は第１，２図によつて説明した従来方式に停電時クロックＣＬ₂、クロック切替回路９を付加するとともに、停電検出信号ＤＥをＩ／Ｏ（入出力装置）４を介してマイクロプロセッサ２で検出できるようにした、つまり停電か否かの判断機能（第４図の流れ図⑦を参照）を持たせるようにしたものである。

すなわち、通電（平常）時においては上述と同様の動作が行なわれるが、停電が停電検出回路５によつて検出されると、該検出信号ＤＥはクロック切替回路９に与えられるので、クロック切替回路９はクロック発生回路１のクロックをＣＬ₁からＣＬ₂に切替える。ここで、通電時クロックＣＬ₁の周期よりも停電時クロックＣＬ₂の周期を長くしておけば、それだけマイクロプロセッサのＷＡＩＴ状態が長くなり、したがつて消費電力を低減することができることになる。さらに、この停電検出信号ＤＥをＩ／Ｏ装置４を介してマイクロプロセッサ２に与えることにより、マイクロプロセッサ２において通電時処理よりも処理時間が短かい停電処理（第３図の⑦′を参照）に切替えるようにすれば、消費電力をより一層低減することができる。なお、その他の点については第１図または第２図の説明と同様であるので省略する。

以上のように、この発明によれば、停電時にはバッテリ補償によつてマイクロプロセッサを動作させ、所定の処理を行わせるようにした制御装置において、より一層の低消費電力化を図ることができるため、従来と同じ時間の停電補償をする場合に、そのバッテリ容量を少なくできる。換言すれば、バッテリ容量が同じであれば停電補償時間を従来よりも長くすることができるものである。

なお、この発明は上記と同様の構成、すなわち停電時に処理装置を動作させる必要のある装置一般に適用可能である。

4. 図面の簡単な説明

第１図はマイクロプロセッサを用いた制御装置の従来例を示すブロック図、第２図は第１図の動

作を説明するための流れ図、第３図はこの発明の実施例を示すブロック図、第４図は第３図の動作を説明するための流れ図である。

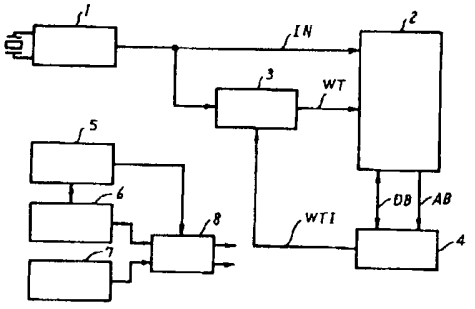
符号説明

１……クロック発生回路、２……マイクロプロセッサ、３……ＷＡＩＴ回路、４……Ｉ／Ｏ（入出力装置）、５……停電検出回路、６……電源回路、７……バッテリ、８……切替回路、９……クロック切替回路、ＩＮ……インタラプト信号、ＷＴ……ＷＡＩＴ（待機）信号、ＷＴＩ……ＷＡＩＴ命令信号、ＤＢ……データバス、ＡＢ……アドレスバス、ＤＥ……停電検出信号、CL_1，CL_2……クロック信号

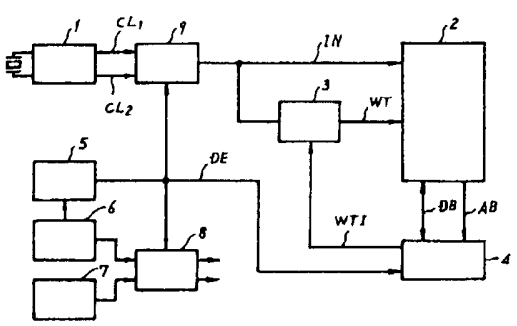
代理人　弁理士　並　木　昭　夫

代理人　弁理士　松　崎　　清

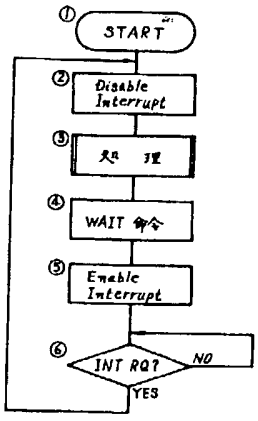
第１図



第３図



第２図



第４図